Performance-Complexity Trade-offs in Millimeter-Wave Transceiver Arrays for Gigabit Mobile Access

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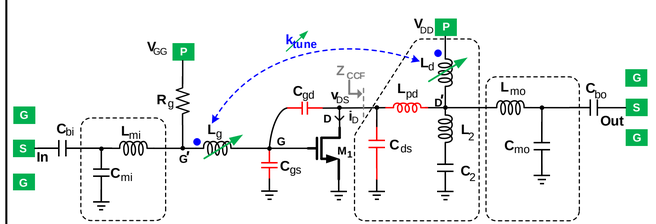
Communication at mmW Frequency

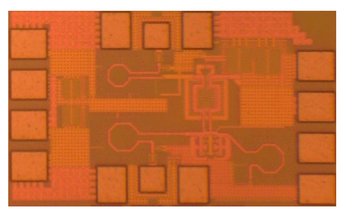
- Global data traffic to grow 7X by 2021 at a CAGR of 47% from 7 Exabytes in 2016 – Cisco Visual Networking Index.
- Multi-Gigabit data-rates possible with large un-congested bandwidths at mmW (27-40G).
- Efficient space-frequency sharing and secure communication with Beamforming.
- Multi-carrier wide-channel BW with complex modulation (for e.g. >64-QAM) is hard to equalize for keeping quadrature & gain flatness.
- Complex modulation schemes can potentially achieves a higher data-rate but are currently limited by dynamic range and power consumption to meet required sensitivities.

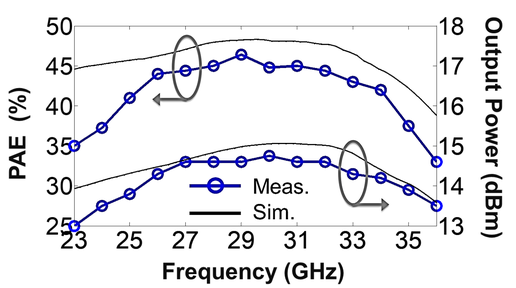
Recent Work at WSU

- Linear and power-efficient 28GHz CMOS PA supporting 512-QAM signal for 5G phased arrays.
- Frequency Reconfigurable CMOS PA with >40% PAE for 28GHz 5G mobile communications.
- V-band sub-harmonic injection-locked beamforming receiver arrays with >11 GHz BW using <15 mW/Ch.
- A 26-34GHz continuous Class-F PA with 46% Peak PAE for MIMO application.
- Several building-blocks for 5G & mmW applications, such as wide tuning range VCOs, wideband LNAs with low-NF, on-chip supply-regulators with high power- and area- efficiency.

Wideband Continuous Class-F CMOS PA

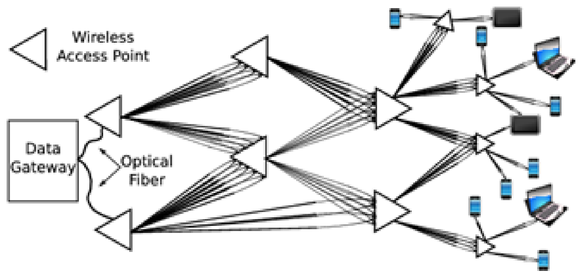


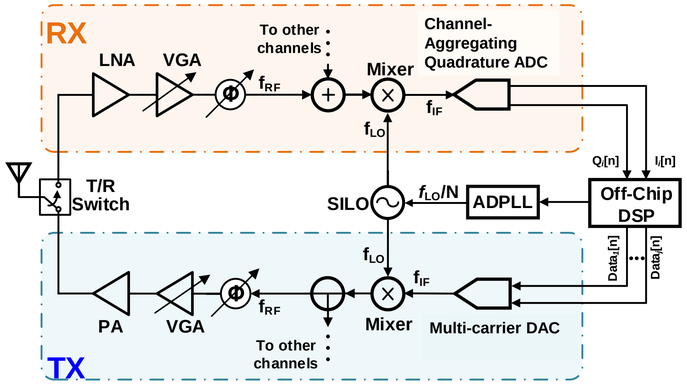




- Highly power-efficient wideband continuous class-F mmW CMOS PA
- Tunable C_{gd} neutralization
- PAE >42% across 26-34GHz
- 65nm CMOS Tech.
- Compact 0.12mm^2 area

Proposed Transceiver Arrays for Gigabit Mobile Access





- Two-level network architecture
- Larger triangles → Access Points that form the backhaul network.
- Smaller triangles → small cell Access Points that provide access to Mobile Stations

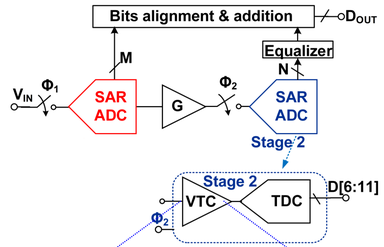
- Beamforming architecture proposed for easier reconfigurability and lower power consumption.

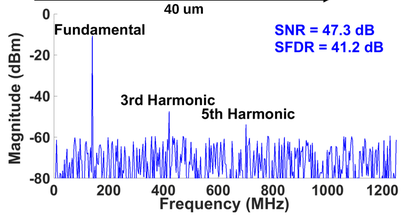
- 16-element array with ability to process higher order modulation schemes up to 512-QAM
- Key innovation in design blocks include:

1) High efficiency PA supporting wide bandwidths.
2) Multi-carrier DAC with noise-cancellation scheme to relax anti-alias filtering with low-power
3) Frequency-interleaved pipeline ADC to support inter-band carrier aggregation
4) Sub-harmonic LO generation with highly linear iterative time-to-digital converter with sub-picosecond resolution.

Proposed Noise-Cancelling ADC

- Lower power consumption, compared to time-interleaved high speed ADCs, makes frequency-interleaving an attractive option in a high speed design.
- Each frequency-interleaved path comprises of two quadrature harmonic-reject mixers with four identical low-pass filters and four sub-ADCs.
- A SAR with a time-based sub-ADC forms the single ADC lane which first converts the residue voltage from previous stage to a time signal through a Voltage to Time Converter.





Conclusions & Future Work

- 4-element 28GHz receiver arrays with >1GHz BW using <20 mW/Ch. and high power- and area- efficient PA.
- Demonstration of complete mmW Front-end design.