**Introduction**

The high speeds and low latency expected in mmWave wireless communications will require strong error correcting codes and efficient decoders. Channel conditions can change widely due to factors such as beam alignment, blockage, and interference; so it will be necessary to probe the channel frequently and adjust the modulation, coding rate, and decoder to the current conditions. Furthermore, some of the common assumptions might no longer be valid, diminishing the generation and quantization of Log-Likelihood Ratios (LLR) for the decoder.

To maximize throughput, the decoder will use all the information available, even corrupted data in packets that failed to decode. We propose incremental redundancy (IR) instead of automatic repeat request (ARQ) for error control. The choice of IR bits will be based on receiver feedback when possible.

**Low Density Parity Check (LDPC) codes offer good performance over a wide range of rates and efficient parallel decoding.** Quasi-cyclic LDPC codes (QC-LDPC) have been of interest in practice since they can be encoded and decoded using feedback shift-registers [1]. The quantization of the LLR values has not been studied when it is to be combined with IR and practical QC-LDPC codes. Our research focuses on the design of LLR quantization and IR schemes for QC-LDPC codes tailored towards mmWave communications. This will require collaboration across multiple research areas: channel characterization for the LLC generation, mmWave tailored towards mmWave conditions. This will require collaboration across multiple research areas: channel characterization for the LLC generation, mmWave tailored towards mmWave conditions.

**Abstract**

Quasi-Cyclic Low Density Parity Check (QC-LDPC) codes offer very good asymptotic performance over a wide range of code rates and efficient parallel decoding, which makes them one of the top candidates for error correction in mmWave communications. However, it is necessary to investigate how practical limitations will impact their performance, and research methods to overcome any degradation that might appear. This poster focuses on the quantization of the LLC values at the decoder input and the effect of incremental redundancy with or without feedback.

The main results in this poster are: 1) spreading the quantization thresholds beyond those maximizing the channel capacity can lower the Frame Error Rate (FER) in the high-SNR regime, 2) QC-LDPC decoders correct error bursts better than random errors, 3) Zerosing small LLCs when the decoding fails can help in the high SNR regime, 4) LLCs can be estimated adaptively based on channel output distribution or number of failed checks, 5) Feedback significantly enhances the benefits of Incremental Redundancy (IR) bits.

**Quantization**

The quantization of LLC values needs to strike a balance between speed and precision. In theory the thresholds should maximize the capacity of the DMC, but these are not always optimal for a Min-Sum decoder with limited precision and iterations. The left plot below shows that spreading these quantization thresholds by 10% reduces FER both with and without IR. This could be related to the assignment of LLC values or with the scaling of extrinsic information in the Sum-Decoder.

Increasing the number of quantization bits provides diminishing returns in raw BER. Incremental redundancy can help bridge the gap left by a coarse A/D, as shown in the right plot below.

**Future research**

Large antenna arrays in mmWave provide narrow beams with strong gains, but beams could get misaligned and it is not possible to have fine A/D converters for each antenna element. Hence, we will seek trade-offs between beamforming, spatial multiplexing, sampling rates, and A/D quantizers.

**References**


