Modeling and Design Techniques for Energy-Efficient and Scalable MIMO Transceivers for Gigabit Mobile Access

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Communication at mmWave Freq

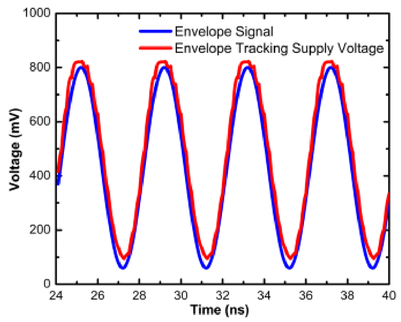
- Global data traffic to grow 10X by 2018 at a CAGR of 61% from 1.5 Exabytes in 2013 – Cisco Visual Networking Index.
- Multi-Gigabit data-rates possible with large un-congested bandwidths at mmWave (64-71G).
- Efficient space-frequency sharing and secure communication with Beamforming.
- Single-carrier wide-channel BW with complex modulation (for e.g. > 16-QAM) is hard to equalize for keeping quadrature & gain flatness.
- Complex modulation schemes can potentially achieves a higher bit rate but are currently limited by dynamic range and power consumption to meet required sensitivities.

Recent Work at WSU

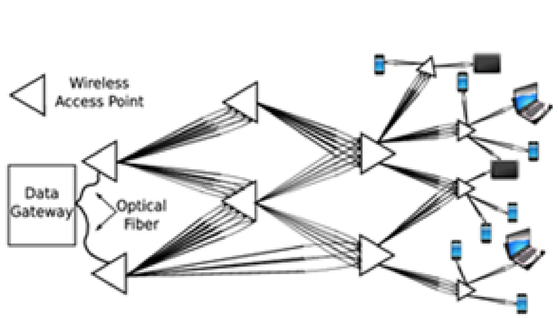
- V-band sub-harmonic injection-locked beamforming receiver arrays with > 11 GHz BW using < 15 mW/Ch.
- Short-range & low-power 60G wireless front-ends achieving ~20Gbps data-rate for Wireless-Network-on-Chips (WiNoCs).
- Several building-blocks for 5G & mmWave applications, such as high-efficiency PAs, wide tuning range VCOs, wideband LNAs with low-NF, low-loss reconfigurable T/R switch, on-chip supply-regulators with high power- and area- efficiency.

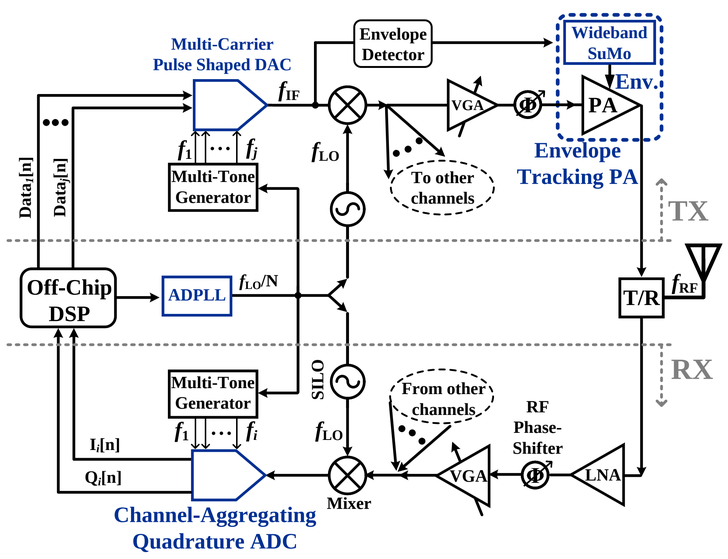
Proposed SuMO for ETPA

- Envelope-tracking CMOS PA for spectrum-efficient high-PAPR data-modulation.
- Novel 0.25GHz BW SuMo using a hybrid topology with dynamic workload partitioning for >10% efficiency improvement.



Proposed Architecture for Access Point Multi-Antenna Receiver





- Two-level network architecture
- Larger triangles → Access Points that form the backhaul network.
- Smaller triangles → small cell Access Points that provide access to Mobile Stations

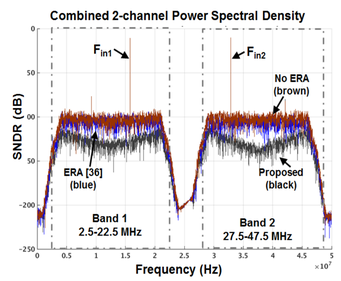
- Hybrid analog/digital beamforming architecture proposed for easier reconfigurability and lower analog power consumption.

- 16-element array with ability to process higher order modulation schemes up to 512-QAM
- Key innovation in design blocks include:

1) High efficiency envelope tracking PA supporting wide channel bandwidths,
2) Multi-carrier DAC with noise-cancellation scheme to relax anti-alias filtering with low-power
3) Frequency-interleaved pipeline ADC to support inter-band carrier aggregation
4) Sub-harmonic LO generation with highly linear iterative time-to-digital converter with sub-picosecond resolution.

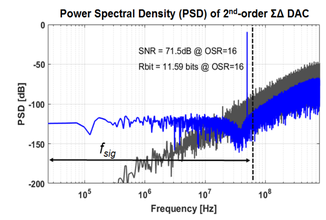
Proposed FI-ADC and Noise-Cancelling DAC

2-channel carrier aggregating Frequency-Interleaved quadrature receiver



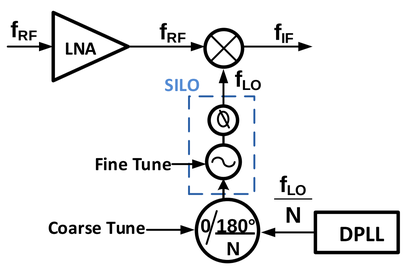
Adaptive LMS calibration to compensate for gain mismatches in parallel channels

Multi-carrier DAC with noise cancellation



Proposed Sub-harmonic LO

- Low-power LO routing.
- No-loss fine-phase-shifting.
- Multiplies up to 9th sub-harmonic.



Conclusions & Future Work

- V-band sub-harmonic injection-locked beamforming receiver arrays with > 11 GHz BW using < 15 mW/Ch. with high power- and area- efficiency.